S2 – Examination 4
Computer Architecture

Duration: 1 hr 30 min

Answer on the answer sheet only.
Do not show any calculation unless you are explicitly asked.
Do not use a pencil or red ink.

Exercise 1 (5 points)

Answer the questions on the answer sheet.

Exercise 2 (4 points)

We want to build a 256-Mib ROM device (labelled ***M***) from several 8-Mib ROM devices (labelled ***m***). The ***M*** device has a 16-bit data bus. The ***m*** devices have a 4-bit data bus. Answer the questions on the answer sheet.

Exercise 3 (4 points)

A microprocessor system includes a ROM device, a RAM device and two peripheral devices (**P1** and **P2**). The capacities (in bits) of these devices are 4 Mib, 256 Kib, 8 Kib and 2 Kib respectively. The microprocessor has a 24-bit address bus (the address bits are numbered from *A0* to *A23* and *A0* is the least significant bit). All the components have an 8-bit data bus. The ROM must be located in the lowest part of the memory space, followed by the RAM, **P1** and **P2**.

1. Calculate the size of the address buses for each device.

For the following questions, the linear-decoding technique must be used.

2. Which address bits are required to select the devices?
3. Write down an expression for each output of the address decoder. Take the *AS* signal (Address Strobe) into account.
4. Give the lowest and highest addresses for each device. (Use the 6-digit hexadecimal representation.)

Exercise 4 (5 points)

A microprocessor system includes a ROM device, a RAM device and two peripheral devices (**P1** and **P2**). The capacities (in bytes) of these devices are 4 KiB, 2 KiB, 1 KiB and 64 bytes respectively. The microprocessor has a 16-bit address bus (the address bits are numbered from *A0* to *A15* and *A0* is the least significant bit). All the components have an 8-bit data bus. The ROM must be located in the lowest part of the memory space, followed by the RAM, **P1** and **P2**.

1. Calculate the size of the address buses for each device.
2. Can we use the linear address decoding?

For the following questions, the block-decoding technique must be used with as few blocks as possible.

3. Which address bits are required to select the devices?
4. Write down an expression for each output of the address decoder. Take the *AS* signal (Address Strobe) into account.
5. Give the lowest and highest addresses for each device. (Use the 4-digit hexadecimal representation.)
6. Work out the number of images for each device.

Exercise 5 (2 points)

A microprocessor system includes a ROM device, a RAM device and two peripheral devices (**P1** and **P2**). The number of address lines of these devices are 23, 21, 15 and 10 respectively. The microprocessor has a 24-bit address bus (the address bits are numbered from *A0* to *A23* and *A0* is the least significant bit). All the components have an 8-bit data bus. The ROM must be located in the lowest part of the memory space (it will start at 0), followed by the RAM, **P1** and **P2**. No empty space should be found between the memory spaces occupied by all the devices.

1. Give the lowest and highest addresses for each device. (Use the 6-digit hexadecimal representation.)
2. Write down **the simplest** expression for each output of the address decoder. Take the *AS* signal (Address Strobe) into account.

Family name: ..... First name: ..... Group: .....

ANSWER SHEET

Exercise 1

Question	**Answer**
A memory has a width of 8 bits and a capacity (in bytes) of 128 KiB. How many address lines does this memory have?	
A memory has a 16-bit data bus and a 16-bit address bus. **In a power of two**, what is the capacity in bits of this memory?	
An **M1** memory has an 8-bit data bus and a 16-bit address bus. Two **M1** memories are connected in parallel to build an **M2** memory. What is the size of the address bus of the **M2** memory?	
A microprocessor has a 20-bit address bus. Six address lines are used for selecting the devices. With the block address decoding, what is the maximum number devices that can be connected to this microprocessor?	
A microprocessor has a 22-bit address bus. Using the linear address decoding, we connect this microprocessor to the four following devices. • a ROM device (15 address lines) • a RAM device (12 address lines) • two peripheral devices (10 address lines) How many address lines are unused in the case of the RAM device?	

Exercise 2

Question	**Answer**
What is the depth of the ***m*** memory?	
What is the depth of the ***M*** memory?	
What is the number of address lines of the ***m*** memory?	
What is the number of address lines of the ***M*** memory?	
How many memory devices should be put in parallel?	
How many memory devices should be put in series?	
How many address lines are required to control the *CS* input of the memory devices?	
When the ***M*** memory is active, how many ***m*** memory devices are active simultaneously?	

Exercise 3

1. ROM: RAM: P1: P2:	2. Device-selection bits:

3. CS_{ROM} =	CS_{P1} =
CS_{RAM} =	CS_{P2} =

4.

Device	**Lowest Address**	**Highest Address**
ROM		
RAM		
P1		
P2		

Exercise 4

1. ROM : RAM : P1 : P2 :	2. Can we use the linear address decoding? (Yes or No)
	3. Device-selection bits:

4. CS_{ROM} =	CS_{P1} =
CS_{RAM} =	CS_{P2} =

Device	5.		6.
	Lowest Address	**Highest Address**	**Number of Images**
ROM			
RAM			
P1			
P2			

Exercise 5

1.

Device	Lowest Address	Highest Address
ROM		
RAM		
P1		
P2		

2.

CS_{ROM} =	CS_{P1} =
CS_{RAM} =	CS_{P2} =

Feel free to use the blank space below if you need to: