S2 – Examination 4
Computer Architecture

Duration: 1 hr

Answer on the answer sheet only.
Do not provide detailed answers or calculations unless you are explicitly asked.
Do not use a pencil or red ink.

Exercise 1 (7 points)

Answer the questions on the answer sheet.

Exercise 2 (5 points)

We want to build a 512-Mib ROM device (labelled ***M***) from several 4-Mib ROM devices (labelled ***m***). The ***M*** device has a 16-bit data bus. The ***m*** devices have an 8-bit data bus. Answer the questions on the answer sheet.

Exercise 3 (5 points)

A microprocessor system includes a ROM device, a RAM device and two peripheral devices (**P1** and **P2**). The capacities (in bytes) of these devices are 128 KiB, 32 KiB, 8 KiB and 256 bytes respectively. The microprocessor has a 20-bit address bus (the address bits are numbered from *A0* to *A19* and *A0* is the least significant bit). All the components have an 8-bit data bus. The ROM must be located in the lowest part of the memory space, followed by the RAM, **P1** and **P2** (the highest addresses will not be used).

1. Calculate the size of the address buses for each device.

For the following questions, the block-decoding technique must be used with as many blocks as possible.

2. Which address bits are required to select the devices?
3. Write down an expression for each output of the address decoder. Take the *AS* signal (Address Strobe) into account.
4. Give the lowest and highest addresses for each device. (Use the 5-digit hexadecimal representation.)
5. Work out the number of images for each device.

Exercise 4 (3 points)

A microprocessor system includes a ROM device, a RAM device and two peripheral devices (**P1** and **P2**). The number of address lines of these devices are 14, 11, 9 and 5 respectively. The microprocessor has a 16-bit address bus (the address bits are numbered from *A0* to *A15* and *A0* is the least significant bit). All the components have an 8-bit data bus. The ROM must be located in the lowest part of the memory space (it will start at 0), followed by the RAM, **P1** and **P2**. No empty space should be found between the memory spaces occupied by all the devices.

1. Give the lowest and highest addresses for each device. (Use the 4-digit hexadecimal representation.)
2. Write down **the simplest** expression for each output of the address decoder. Take the *AS* signal (Address Strobe) into account.

Family Name ..... First Name ..... Class.....UID.....

ANSWER SHEET

Exercise 1

Question	Answer
If a memory has a width of 8 bits, is its capacity in bytes equal to its depth?	
A memory has a width of 16 bits and a capacity of 128 Kib. How many address lines does this memory have?	
A memory has a 32-bit data bus and a 16-bit address bus. **In a power of two**, what is the capacity in bytes of this memory?	
An **M1** memory has an 8-bit data bus and a 16-bit address bus. Two **M1** memories are connected in series to build an **M2** memory. What is the size of the address bus of the **M2** memory?	
A microprocessor has a 20-bit address bus. The largest device connected to this microprocessor has 17 address lines.. With the block address decoding, what is the maximum number devices that can be connected to this microprocessor?	
A microprocessor has a 22-bit address bus. Using the block address decoding, we connect this microprocessor to the four following devices. • a ROM device (20 address lines) • a RAM device (12 address lines) • two peripheral devices (10 address lines) Can a fifth component be connected to this microprocessor?	
A microprocessor has a 22-bit address bus. Using the block address decoding, we connect this microprocessor to the four following devices. • a ROM device (20 address lines) • a RAM device (12 address lines) • two peripheral devices (10 address lines) How many address lines are unused in the case of the RAM device?	

Exercise 2

Question	**Answer**
In a power of two, what is the depth of the ***m*** memory (the number of words)?	
In a power of two, what is the depth of the ***M*** memory (the number of words)?	
What is the number of address lines of the ***m*** memory?	
What is the number of address lines of the ***M*** memory?	
How many memory devices should be put in parallel?	
How many memory devices should be put in series?	
How many address lines are required to control the *CS* input of the memory devices?	
When the ***M*** memory is active, how many ***m*** memory devices are active simultaneously?	

Exercise 3

1. ROM : RAM : P1 : P2 :	2. Device-selection bits:

3. CS_{ROM} =	CS_{P1} =
CS_{RAM} =	CS_{P2} =

Device	4.		5.
	Lowest Address	**Highest Address**	**Number of Images**
ROM			
RAM			
P1			
P2			

Exercise 4

1.

Device	Lowest Address	Highest Address
ROM		
RAM		
P1		
P2		

2.

CS_{ROM} =	CS_{P1} =
CS_{RAM} =	CS_{P2} =

Feel free to use the blank space below if you need to: